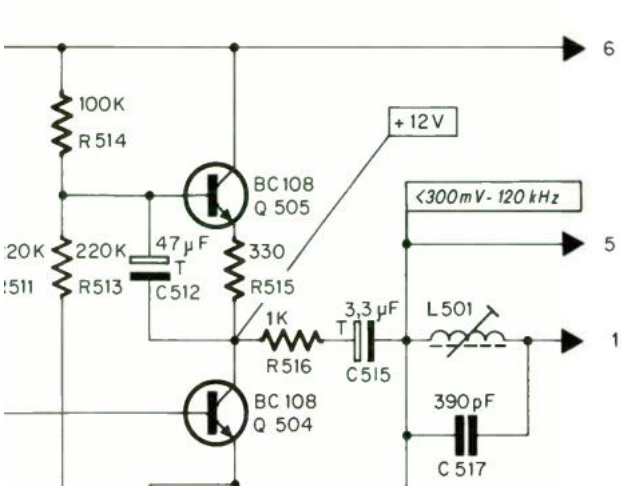
Revox A77 Record Amplifier — 120 kHz Bias Trap Sweep

The Record Amplifier of the Revox A77 (assembly 1.077.705) includes a parallel LC "trap" - L501/C517 - whose job is keeping the tape recorder's ~120 kHz bias oscillator signal out of the record amplifier's output. This report simulates that trap in LTspice and compares three candidate capacitor values to see which one places the notch closest to the bias frequency.

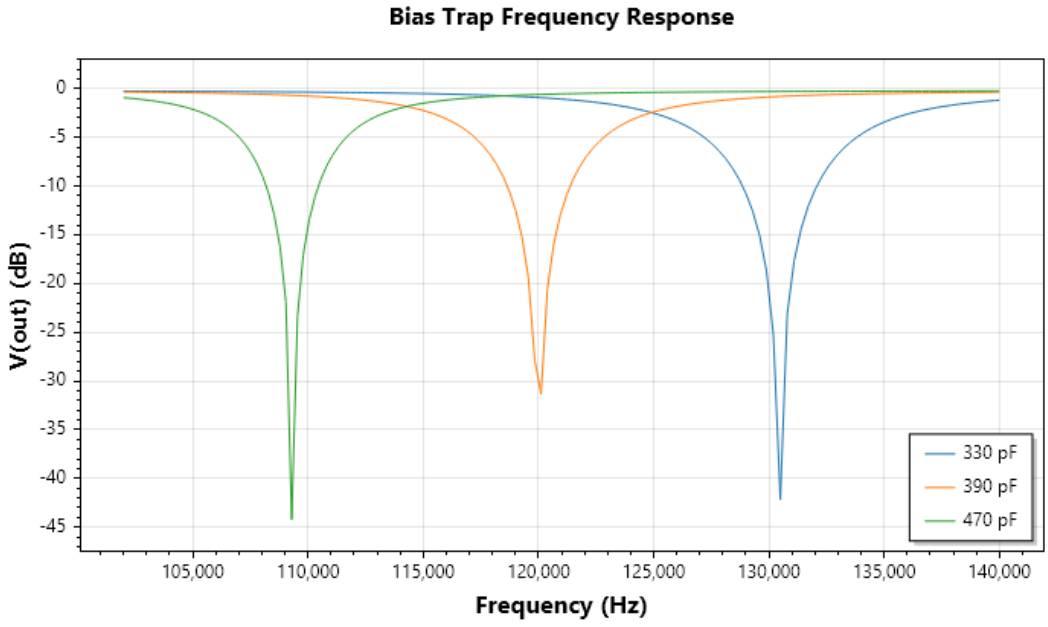


Record amplifier bias trap section - L501/C517 - from the Revox A77 service manual, annotated with the spec it has to meet: less than 300 mV at 120 kHz.

The circuit and the sweep

```
* Revox A77 Record Amplifier (1.077.705) - 120 kHz Bias Trap Parameter Sweep

* Define base parameters
.param C_val=390p
.param L_val=4.51m

* Input voltage source
V1 in 0 AC 1

* Source resistance
Rs in trap_in 1k

* Parallel LC Bias Trap with variable parameters
L501 trap_in out {L_val}
C517 trap_in out {C_val}

* Load resistance
Rl out 0 50k

* AC Analysis
.ac dec 1000 102k 140k

* Step capacitance using a list of standard values
.step param C_val list 330p 390p 470p

* Step inductance linearly (e.g., core tuning from 4.3 mH to 4.7 mH with 0.1 mH
step)
* To sweep L_val, uncomment the following line:
* .step param L_val 4.3m 4.7m 0.1m
```

Frequency response



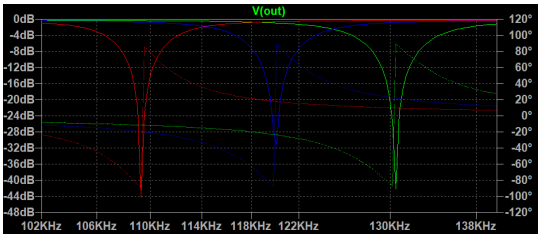
How this report was built

The three stepped curves above started out as three separate, auto-generated charts: MD Visor's

Create Report from CSV wizard reads an LTspice ".step" export directly, recognizing the "Step Information: ..." markers LTspice writes between runs and turning them into one wide table - `trap_multi.txt` was added to the wizard three times, picking one capacitor value's column each time. That gave a basic report with one chart per value.

Combining all three into the single comparison chart above - and everything else on this page, including this section, the schematic, and the conclusions - was then done by hand-editing the generated Markdown: merging the three `y:` columns into one chart block, adding a legend and axis labels, and writing up what the result actually means. This is the intended workflow for the wizard: it gets the data in and gives you something to look at immediately, and you take it from there.

LTspice's own plot, for comparison



LTspice's own overlay of all three ".step" runs - magnitude (solid) and phase (dotted) - shown here to confirm the chart above matches the simulator's own output.

Conclusions

The simulated notch frequency for each capacitor value:

C_val	Notch frequency	Notch depth
330 pF	~130.5 kHz	-42.2 dB
390 pF	~120.1 kHz	-31.3 dB
470 pF	~109.3 kHz	-44.2 dB

390 pF - the netlist's own default value - places the notch almost exactly on the 120 kHz bias frequency the schematic calls out, which is why it's the value actually used in production. 330 pF and 470 pF both give a deeper notch, but centered well off the bias frequency, which would leave more bias signal getting through than the shallower-but-correctly-centered 390 pF trap.